CLAIMS:

1. Method for reducing power dissipation in a power amplifier for use in wireless communication systems, said power amplifier having transistors showing a quiescent current, wherein the quiescent current of the power amplifier is adaptively changed according to the average output power of the power amplifier.

2. The method of claim 1, wherein the adaptive biasing of the power amplifier having at least two stages, is done by changing the value of I_Q of at least one of the stages of the power amplifier.

3. The method of claim 1, wherein the adaptive biasing of the power amplifier having at least two stages, is done by changing the value of I_Q of all the stages of the power amplifier.

4. The method of claim 1, wherein the adaptive biasing of the power amplifier having at least two stages, is done by changing the value of I_Q of the power stage of the power amplifier.

5. The method of any of the claims 1 to 4, wherein the adaptive biasing of the power amplifier having at least two stages, is done by detecting the average output power of the power amplifier in a power detector and varying the value of I_Q of the two stages according to the detected power and a specified function of an adaptive biasing circuit.

6. The method of any of the claims 1 to 5, wherein a voltage or current quantity proportional to the average output power is detected as average output power of the power amplifier.

7. The method of any of the claims 1 to 6, wherein a voltage or current quantity proportional to the average output power is detected in any of the stages of the power amplifier, preferably in a driver stage of the power amplifier.

8. The method of claim 5, wherein the average output power is detected by applying a squaring function and averaging a scaled copy of the collector current of the driver and/or power stage.

9. The method of claim 8, wherein the averaging function is carried out directly after the squaring function in the power detector.

10. The method of claim 8, wherein the averaging function is carried out in the adaptive biasing circuit.

11. A power amplifier for use in wireless communication systems, said power amplifier having transistors showing a quiescent current, comprising adaptive biasing means changing the quiescent current of the power amplifier according to the average output power of the power amplifier for reducing power dissipation in the power amplifier.

12. The power amplifier of claim 11, wherein the adaptive biasing means comprise a power detector detecting a quantity proportional the output power of the power amplifier and a adaptive biasing circuit.

13. The power amplifier of claim 12, wherein the power detector is configured to provide a squaring function and an averaging function on a quantity proportional to the output power of the power amplifier.

14. The power amplifier of claim 12, comprising a driver stage, a current biasing network connected to the driver stage, an intermediate matching network, a power stage, and a current biasing network connected to the power stage, wherein the power detector is connected to an input of the driver stage, and the adaptive biasing circuit is connected to the input of the power stage.

15. The power amplifier of claim 12, wherein the adaptive biasing circuit comprises a processing block connected to the power detector, and a current biasing network connected between the processing block and the input of the power stage.

16. The power amplifier of claim 15, wherein the processing block comprises an analog-to-digital converter, a look-up table providing the function of changing the quiescent current of the power amplifier according to the average output power of the power amplifier, and a digital-to-analog converter.

17. The power amplifier of claim 15, wherein the processing block comprises a differential analog circuit implementing the function:

$$P_{DC}(I_Q) = \min I_Q (P_{DC}) \text{ with } \Delta G < \Delta G_{max} \text{ and spec (linearity)}$$

where ΔG is the gain variation and ΔG_{max} is the maximum gain variation allowed by the application, and the spec (linearity) is the linearity specification for the application

18. The power amplifier of claim 15, wherein the processing block comprises an analog implementation circuit where a difference of $I_{pow} = I_{sq} - I_{ref}$ is calculated in the current domain and averaging is performed by a capacitor connected between a node carrying I_{pow} and ground.

19. The power amplifier of claim 18, wherein a diode stage is connected between a node carrying I_{pow} and ground.

20. The power amplifier of claim 18, wherein a resistor is connected between a node carrying I_{pow} and a mirror circuit provided at the output of the processing block and outputting I_{out}.

21. A UMTS hand set comprising a power amplifier configured as claimed in any of the claims 11 to 20.